## 13.7 A Reconfigurable Sense Amplifier with Auto-Zero Calibration and Pre-Amplification in 28nm CMOS

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High-performance SRAMs are critical elements in microprocessors and SoCs. Fast and robust bitline sensing is a key requirement in such memories. With process scaling, increased mismatch in the sense amplifier (SA) circuit and increased $I_{read}$ variation in the bitcell [1] have degraded sensing robustness. The fundamental tradeoff between sensing time and bitline read failures (Fig. 13.7.1) forces designers to heavily margin sensing time in order to guarantee sufficient bitline differential voltage prior to SA triggering. Previous research has improved SA robustness using pre-amplification circuits [2], capacitance-based offset cancellation [3-4], and redundancy [5]. However, most of these schemes target single-ended sensing (losing the benefit of common-mode rejection), incurring up to 60% area overhead or post-silicon tuning costs.

This work presents an area-efficient and variation-tolerant small-signal differential sensing (VTS) scheme that modifies the conventional SA circuit to include: 1) a structure for on-the-fly, auto-zeroing offset compensation, 2) pre-amplification of bitline differential by reconfiguring the SA inverter pair as amplifiers, and 3) latching of the amplified voltage differential by returning the SA to its conventional cross-coupled configuration. The approach is demonstrated to improve SA robustness over conventional sensing at iso-sensing time without area overhead (Fig. 13.7.1). Conversely, sensing time can be reduced at iso-robustness and area. Measurements of a 28nm CMOS test chip show that an iso-area VTS scheme improves offset noise tolerance by ~1.2$\sigma_{Vth}$ or sensing speed by up to 42% at iso-robustness (<0.3% failure rate).

The VTS scheme reconfigures the inverter pair of the SA, effectively putting it to use during all phases of operation to provide offset cancellation and additional amplification (Fig. 13.7.1): 1) During bitline precharge, the SA does not have to detect bitline droop allowing the inverters to be decoupled from each other and biased in their high-gain regions close to their ideal trip-points. AC-coupling capacitors C1 and C2 enable independent biasing of the bitlines and inverters. In addition, the capacitors also compensate for mismatch in the inverter trip-points via auto-zeroing. 2) During reads, the bitcell wordline is activated and the inverters function as offset-compensated pre-amplifiers for the bitline differential (in contrast to conventional SAs, where they remain idle). 3) Finally, the inverters are cross-coupled to further amplify and latch the data using regenerative feedback, as in a conventional SA.

Figure 13.7.2 shows the circuit schematic of the VTS-SA. The 2:1 bitline mux, precharge and output driver circuits are similar to those in the conventional SA. The 10-T reconfigurable inverter circuits are coupled to the multiplexed bitlines using capacitors $C_{MOM1}$ and $C_{MOM2}$. Transistors M3-4 and M5-6 form the SA inverters and NMOS switches M7-10 are used to reconfigure inverter connections for auto-zeroing, pre-amplification, and latching modes. NMOS switches M11 and M12 isolate the MOM capacitors during regeneration, preventing full rail voltage swing at nodes BL_MX/BL_MX_B that could turn on bitline mux switches and severely degrade performance. Since this scheme incorporates automatic offset compensation, the SA is not highly sensitive to mismatch. Hence, all devices in the VTS-SA are near minimum-sized and can leverage density improvements from technology scaling. This is in contrast to conventional SAs, which require large devices to reduce mismatch and therefore have not tracked with feature size improvements [6].

Figure 13.7.2 also shows simulated waveforms for the selected bitlines and SA inverter outputs through various phases of operation. During biasing/offset storage, the input and output of the SA inverters are shorted together, which creates a 14μA (measured) short-circuit current that would increase power consumption in this scheme. However, biasing and offset storage require only ~60% of the precharge phase to complete and are therefore duty-cycled, resulting in 26% measured SA power savings (compared to no duty-cycling). Headers and footers for duty cycling are shared across 16 SAs. During the bitcell read phase, the capacitors connect the bitlines to the inverter inputs while their outputs are disconnected. This compensates for inverter trip-point offset and enables pre-amplification of bitline droop (~3.2× larger bitline swing at 60ps sensing time, simulated at TT corner, 1V, and 27°C). Finally, the inverters are cross-coupled when SA_EN is enabled for latching.

$C_{MOM1}/C_{MOM2}$ size is a critical design parameter in the VTS scheme. Increasing these capacitances degrades sensing time (due to larger bitline capacitance) and requires upsizing of the inverter transistors (M3–M6) to charge the capacitors within a given precharge time. In contrast, smaller capacitors result in reduced coupling, attenuating the input bitline swing and negating the benefit of pre-amplification. Figure 13.7.3 shows the simulated design-space that was used to determine capacitor size. In the test-chip implementation, ~5fF capacitors are used to maximize gain-bandwidth product, striking a balance between coupling ratio and total bitline capacitance while minimizing area. The capacitors are implemented as 7.8×0.76μm$^2$ metal-oxide-metal (MOM) devices, rather than: 1) metal-insulator-metal (MIM) capacitors, that have larger minimum size constraints, or 2) metal-oxide-semiconductor (MOS) capacitors, that undergo weak inversion during auto-zeroing, increasing coupling loss.

The VTS-SA is implemented in an 8kb SRAM array composed of high-density 6T bitcells (Fig. 13.7.3). The bitlines are interleaved 2:1 with 128 bits on each column. The MOM capacitors are pitch-matched to the SA and placed on top of two bitcell columns in metals 5 and 6. Figure 13.7.3 also shows the timing diagram for read-control signals in the VTS scheme. To evaluate robustness and speed improvements, a conventional SA-based array is also implemented, where the SA is sized for 4.5$\sigma$ yield and has an area of 4.62μm$^2$. Placing the MOM capacitors over the bitcells and using near-minimum sized devices enables an iso-area implementation of the VTS-SA, despite 2× higher transistor count. Because of the additional 2 routing layers used by the MOM capacitor placement strategy, it may not be feasible in some routing-resource-limited cases (e.g., generic memory compilers). However, custom memory design applications such as processors often have sufficient (≥ 9) metal layers where a similar implementation can be achieved with little impact on overall routing.

The test harness used to characterize the SAs is shown in Fig. 13.7.4. The arrays are programmed with pseudo-random data using a 32b LFSR. To measure sensing speed, the WL_EN to SA_EN delay is swept using a two-stage delay chain and any read failures are recorded over $2^{32}$ experiments operating at 1.8GHz. Similarly, SA robustness (offset noise tolerance) is characterized by skewing the supply voltages of the cross-coupled inverters (to induce mismatch) at a fixed nominal sensing time. Figure 13.7.5 shows measured SA sensing speed and robustness characterization for conventional and VTS implementations across 22 dice. For a typical die, VTS improves sensing speed by 34% over conventional sensing at a fixed read failure rate (<0.3%). Alternatively, this corresponds to ~0.9$\sigma_{Vth}$ higher offset noise tolerance. Across dice, sensing-speed improvements range from 25% to 42%, corresponding to robustness improvements of 0.6$\sigma_{Vth}$ to 1.2$\sigma_{Vth}$ (Fig. 13.7.6). Figure 13.7.6 also shows that VTS-based sensing-speed improvement is relatively stable across temperatures. The table in Fig. 13.7.6 compares the key characteristics of VTS and conventional sensing approaches.

*Acknowledgements:*
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*References:*
[1] J. Wang, *et al.*, "Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory using Voltage Acceleration Method," *IEEE Symp. VLSI Technology*, pp. 220-221, 2011.
[2] D. Schinkel, *et al.*, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC Dig. Tech. Papers*, pp. 314-315, 2007.
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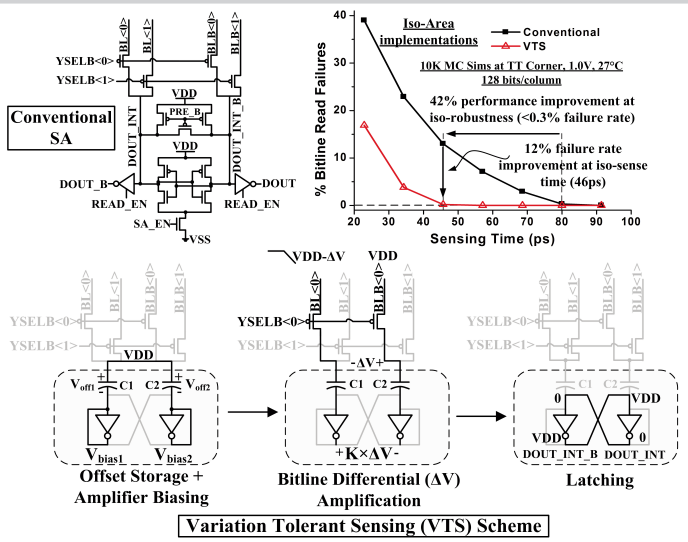



Figure 13.7.1: High-level operation of VTS and its sensing speed/robustness advantage over conventional sensing (simulated).

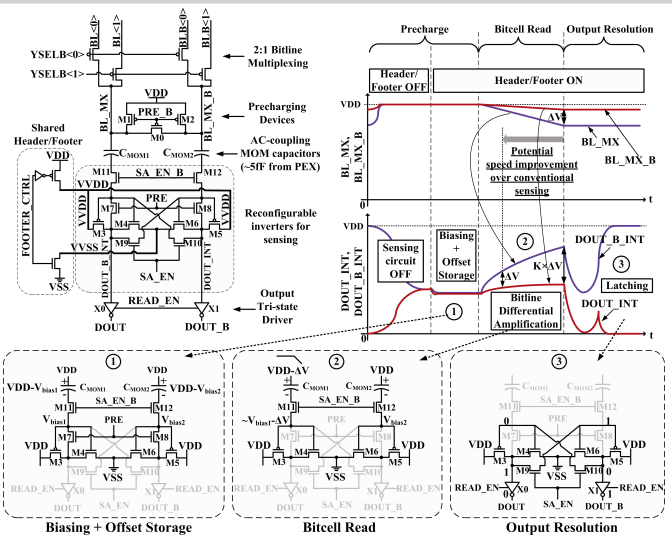



Figure 13.7.2: VTS-SA circuit schematic and operation phases showing relevant waveforms and circuit configuration in each phase.

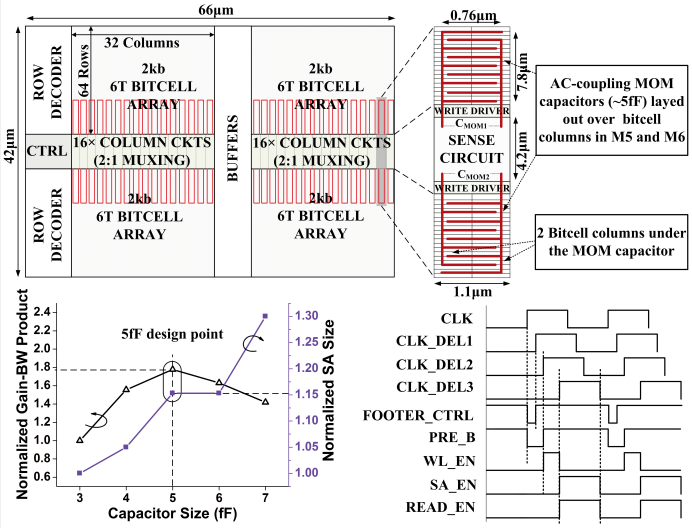



Figure 13.7.3: 8kb SRAM array with VTS showing capacitor placement strategy. Simulated capacitor sizing design space and VTS read timing.

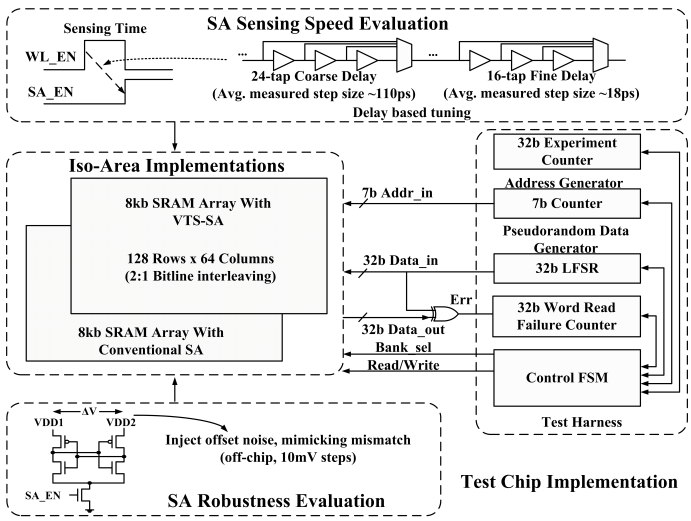



Figure 13.7.4: Test-chip implementation to characterize SA sensing speed and robustness.

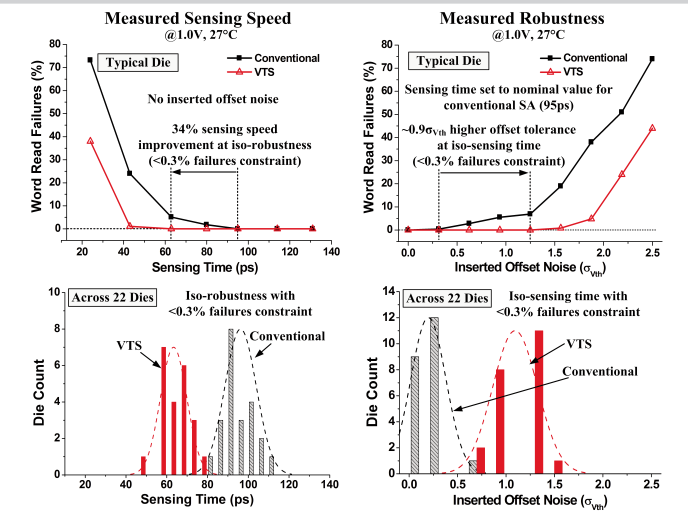
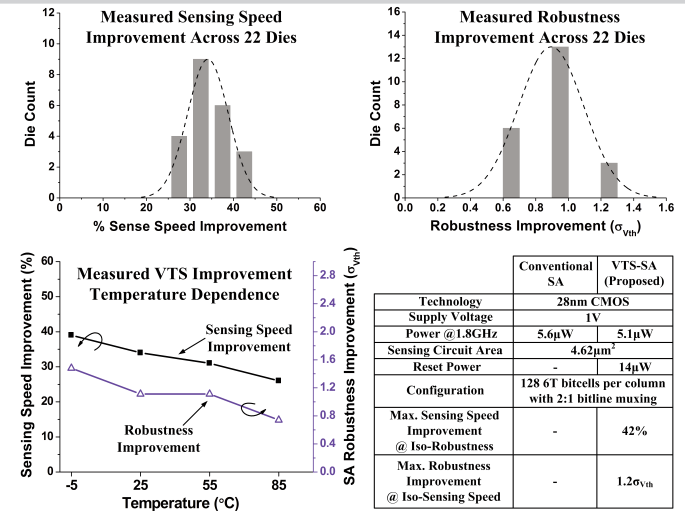



Figure 13.7.5: Measured SA sensing speed and robustness for VTS and conventional implementations. For a typical die, VTS improves sensing speed by 34% (corresponding to $0.9\sigma_{Vth}$ higher offset noise tolerance).




| | Conventional SA | VTS-SA (Proposed) |
|---|---|---|
| Technology | 28nm CMOS | |
| Supply Voltage | 1V | |
| Power @1.8GHz | 5.6µW | 5.1µW |
| Sensing Circuit Area | 4.62µm² | |
| Reset Power | - | 14µW |
| Configuration | 128 6T bitcells per column with 2:1 bitline muxing | |
| Max. Sensing Speed Improvement @ Iso-Robustness | - | 42% |
| Max. Robustness Improvement @ Iso-Sensing Speed | - | $1.2\sigma_{Vth}$ |

Figure 13.7.6: Measured VTS-SA sensing speed and robustness improvements across 22 dice. Measured temperature dependence of VTS improvement and comparison summary.

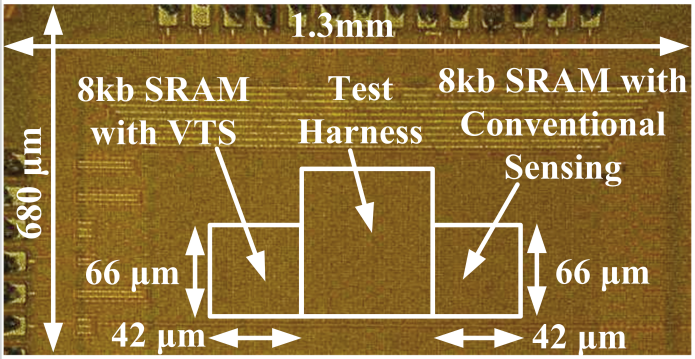



Figure 13.7.7: Die micrograph in 28nm CMOS.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