A Test Platform for the Thermal, Electrical, and Mechanical Characterization of Packages

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Abstract

As packages become more complex with increasing power and thermal demands, a test platform that combines many aspects of package characterization simplifies the prototyping of new packages. The test platform is embodied in a chip called the Package Killer Chip (PKC). PKC is a 188 mm^2 chip with a maximum power dissipation of 355 W from a 1.8 V power supply. PKC has 3944 unit cells, each with individually programmable heaters to dissipate power, and circuits to measure the local temperature and power supply voltages with a 180 µm resolution. Dynamic loads can be generated by cycling through four power profiles stored on-chip at up to 1 GHz. Power supply transients due to dynamic loads can be measured and visualized using on-chip samplers. Chip orientation relative to a package or adjacent chip in a multi-chip module (MCM) can be measured using on-chip alignment sensors. A three-chip prototype proximity communication MCM containing two PKC dice and a bridge chip was used to evaluate PKC as a test platform.

Key words: thermal, electrical, mechanical, package, characterization, proximity

1. Introduction

The thermal and electrical requirements of high performance VLSI systems are demanding increasingly complex packages. For example, high-capacity memories often consist of multiple stacked dice and some high-end microprocessors combine two separate processor dice in a single package. Proximity communication (PxC) is a chip-to-chip interconnect technology being developed by Sun Microsystems that enables such multi-chip modules (MCMs) with inter-chip communication performance approaching that of on-chip communication [1]. However, an MCM using PxC requires that its chips be aligned with micron-scale precision [2]. The test platform presented here was motivated by the requirements of proximity communication, but its functionality is applicable to a wide variety of package development.

The test platform, known as the Package Killer Chip (PKC), is able to perform thermal, electrical, and mechanical characterization of packages. Other thermal test chips exist ([3], [4]), but PKC is unique in the granularity and variety of characterizations available on a single die. PKC can present a static thermal/power load and perform static temperature, voltage, and position measurements. Additionally, PKC can be programmed with a time-varying load and can dynamically sample the power supply transient voltages. Targeting a single type of test chip that is able to perform a wide variety of characterizations simplifies initial package development where each package redesign is costly and yields are low.

PKC is meant to mimic a high performance microprocessor. It measures 15 mm x 12.5 mm and is capable of dissipating 355 W from a 1.8 V power supply. As shown in Figure 1, the majority of the chip is covered with a grid of 3944 unit cells, each 180 µm x 180 µm. Each unit cell contains heaters, a CMOS thermometer, and static VDD and GND measurement circuits. The power draw of each unit cell is programmable from 0 to 90 mW. Four power profiles can be stored in each unit cell and cycled at up to 1 GHz to create dynamic loads. The power profiles can be used to emulate the activation of a CPU core or a functional unit, for example. Nine subsampling circuits distributed evenly across the chip measure dynamic transients on the VDD supply.

An important metric of the overall reliability of a package as well as its suitability for 3D integration is its ability to align chips, both to the

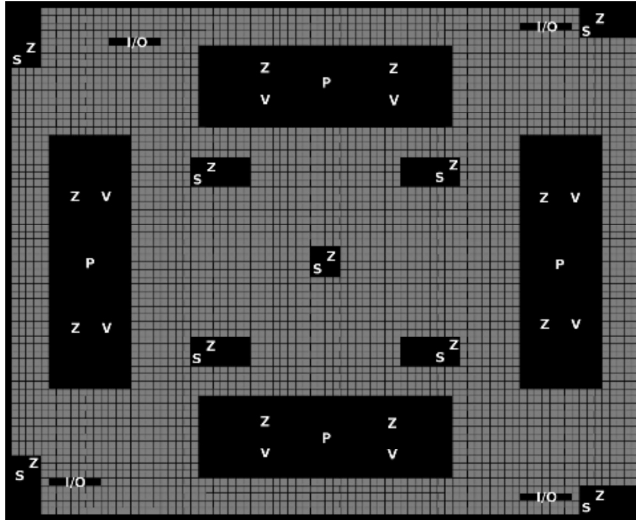

Figure 1. Map of structures on PKC. Gray indicates the grid of unit cells and black is the absence of unit cells. S = sampler, Z = Z-measurement, V = vernier pair, P = proximity, I/O = I/O test.

package as well as to each other, under thermal cycles and mechanical loads. PKC has 17 position measurement structures evenly distributed across the chip that determine chip-to-package or chip-to-chip alignment normal to the plane of the chip (Z-separation and tilt angles) with micron-scale accuracy. Eight additional sensors distributed around the chip's perimeter determine its alignment to neighboring chips of a package in all six degrees of freedom with micron-scale accuracy by combining Z-separation sensors with translational and rotational sensors known as verniers [5].

PKC was fabricated in a TSMC 0.18 µm process with six metal layers and a 1.8 V nominal power supply. Two PKC chips were packaged with a third “bridge” chip in a proximity communication configuration for testing [6]. The chips are reflowed to an alumina ceramic LGA (land grid array) substrate. A cold plate is attached to the chips and coupled to a water cooling system to permit high-power testing.

2. Characterization Features

The capabilities of the various measurement circuits on PKC are detailed in the following sections.

2.1. Unit Cell

The unit cell is the basic building block of PKC. Each of the 3944 unit cells contains heaters, a CMOS thermometer, and static VDD and GND measurement as described in the following sections. A 4-stage shift register in each unit cell stores the power profiles for that cell. Additionally, each unit cell has a bonding site that can accommodate wire bonds, C4 bumps, or other I/O technologies, depending on the final chip fabrication steps. Of the unit cells on PKC, 3863 are either VDD or GND bonding sites due to the power demands of large thermal loads. The remaining unit cells are chip I/O bonding sites. The unit cells are on a 180 µm x 180 µm pitch which is convenient for bonding while allowing for static measurements at a very fine resolution.

2.2. Heater

Each unit cell has three NMOS devices of varying widths that act as the heating elements. The devices short VDD and GND and are sized for nominal drain currents of 5, 15, and 30 mA, respectively. The heaters can be activated individually or in combination for total programmable currents of 0, 5, 15, or 50 mA corresponding to 0, 9, 27, or 90 mW from a 1.8 V VDD. The heater current is individually programmable in each unit cell allowing full-chip heating profiles that emulate hot spots, gradients, or other load patterns. Two control bits indicate which devices to activate. The effective power density is up to 2.8 W/mm^2. Recent high-performance microprocessors have processor core power densities up to 0.7 W/mm^2 and may have hot spots that are higher density [7].

2.3. Heater Shift Register

Each unit cell contains a 4-stage, 2-bit shift register used to store four power settings for that cell. In order to program the chip with a power profile, the shift register is loaded via a scan chain prior to testing. The shift register can be clocked up to 1 GHz, allowing dynamic heater profiles that change up to once per nanosecond. The heater profiles cycle through the four states leading to a periodic, dynamic heat profile that has a period four times that of the shift register clock. The shift register clock was designed to have less than 20 ps of skew, so the heater patterns shift nearly simultaneously everywhere on the chip.

2.4. CMOS Thermometer

The CMOS thermometer in each unit cell is constructed from a vertical PNP device. In a vertical PNP, the grounded P-type substrate is used as the collector, an N-well as the base, and a P$^+$ region as the emitter. For a constant emitter current, I_{BE}, the

emitter voltage, V_{BE}, of the device is directly proportional to absolute temperature according to:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{BE}}{I_{0E}} + 1\right) \quad (1)$$

where k is Boltzmann's constant, q is the electronic charge, and I_{0E} is the saturation current. Exploiting this effect, we determine the temperature in the vicinity of the PNP by forcing a constant 100 μA current into the emitter from off-chip and measuring the V_{BE} of the device.

Outputs of the temperature sensors are multiplexed to a single external output pin, so one unit cell is measured at a time. The temperature sensors are individually activated via a scan chain.

2.5. Static VDD and GND Measurement

Static VDD and GND measurements are provided by tapping into the power grid in each unit cell through a switch. When the switch is connected, it creates a high-impedance signal path that allows direct measurement of the local supply voltage off-chip. The high-impedance path ensures little power supply current flows to the measuring equipment, so there is little voltage drop along the measurement path. This technique allows accurate static measurements, but filters out high-frequency transients. Like the thermometers, the VDD and GND measurements share a common output pin, so they are activated one at a time via a scan chain.

2.6. Power Supply Sampler

The periodic nature of the dynamic loads described in Section 2.3 allows the use of subsampling to observe transients on the VDD power supply. A schematic of one of the nine samplers distributed across the chip is shown in Figure 2. The sampler is essentially an analog flip-flop that captures the same point of the periodic power supply each cycle until the sampler output stabilizes. The sample clock runs at ¼ the speed of the heater shift register clock so that the same point is captured each dynamic load profile period. After the sampler output stabilizes and is recorded off-chip, the relative phases of the sample and heater clocks are adjusted to sample a new point on the transient power supply waveform. This is repeated as the relative phase difference is swept across the entire dynamic load period. The bandwidth of observable supply transients is limited by the internal bandwidth of the passgate sampler, which is in the tens of GHz, rather than the output bandwidth because the output is essentially DC [8].

The samplers have their own power supply so that their operation will not be affected by noise

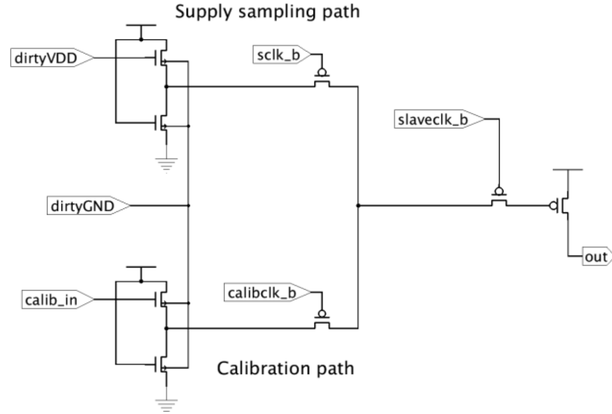

Figure 2. Simplified schematic of power supply sampler. *dirtyVDD* is the supply being sampled. *dirtyGND* is the PKC GND power supply. The sampler uses PMOS devices to ensure a clean supply on the body terminal.

on the main supplies. The samplers can sample a range of voltages from VDD-200 mV to VDD+400 mV, corresponding to voltages from 1.6 V to 2.2 V at nominal VDD. Each sampler has a separate, parallel input path for calibration and must be calibrated prior to first use due to device and process variations.

2.7. Z-separation Measurement

The Z-separation measurement indicates the orthogonal distance between PKC and either the package or a neighboring chip. The measurement is accomplished by determining the capacitance between a metal plate on PKC and a corresponding one on the package or neighboring chip, as described in [5]. The measured capacitance is compared to 3D field solver simulations to determine the *in situ* separation with micron-scale accuracy. There are a total of 17 Z-separation sensors distributed across the chip. The readings from multiple sensors can be compared to determine the tilt angles (out of plane rotations) between PKC and the package or neighboring chip.

2.8. Verniers

The remaining three degrees of mechanical position, X and Y translation and in-plane rotation, are measured using verniers as described in [5] and [9]. A pair of vernier structures placed orthogonally on PKC allows measurement of translation and rotation relative to a package or neighboring chip with similar structures, to micron-scale accuracy. Eight vernier pairs are distributed along the perimeter of the chip.

2.9. I/O Characterization

There are four I/O structure characterization sites on PKC, one in each corner of the chip. Each site contains circuits for performing four-wire resistance measurements of three I/O structures, such as a C4 bump, wire bond, or experimental structure. In addition, at each location there are two I/O sites connected in a loopback fashion to determine the frequency response of I/O structures. These structures are particularly useful if novel I/O structures are being prototyped.

2.10. Proximity Communication (PxC)

Along each edge of PKC is a PxC interface similar to that in [10]. However, only one transmit and one receive channel are activated in each interface. This permits the characterization of a high-speed PxC link to an adjacent chip in an MCM.

3. Testing

PKC was tested in a PxC configuration using three chips in an MCM. Two of the dice are PKCs yielding a theoretical maximum package power dissipation of over 700 W. Activating a single PKC die at full power resulted in solder reflow; however, we were able to obtain reasonable measurements with a maximum power dissipation step size of 0 to 106 W in a single 2 ns period. The limiting factor for maximum power dissipation was the quality of contact between the PKC dice and the heat sink.

The testing results presented in the following sections indicate the effectiveness of PKC as a general package characterization test platform.

3.1. Test Package

The package used in testing, code-named Krazo, is depicted in Figure 3. It is an MCM with three chips arranged in a PxC configuration. The substrate is 45 mm x 45 mm with 1368 LGA pads on a 1.12 mm pitch and is made of alumina ceramic with tungsten interconnect. Two PKC dice are flip-chip bonded to the substrate. The PKC dice are connected through a third bridge chip that is oriented face-up and wire bonded to the substrate. The bridge chip is located in a cavity in the top side of the substrate. This configuration allows all chips to be powered through the substrate while enabling proximity communication through the face-to-face PKC-to-bridge connections. The results presented below are from one of the PKC dice.

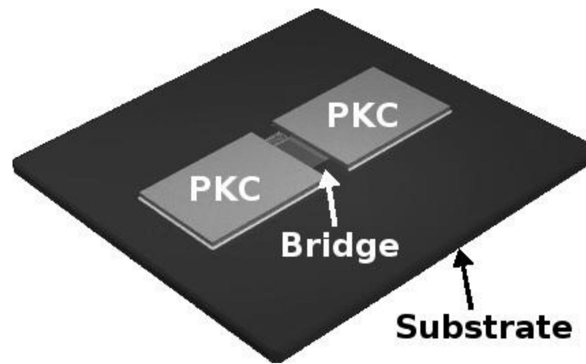

Figure 3. Krazo package.

3.2. Test Setup

The Krazo test setup consists of the hardware and software necessary to provide power and connectivity, as well as the user interface to interact with the unit under test. Elements of this system include a Java-based test infrastructure, GUI, and application code, as well as a custom motherboard. Each die in the package is controlled through a JTAG interface, and a custom clamp mates the board/socket/package stackup. An independent suspension is provided for the microchannel cold plate, which is connected to a thermostatically controlled chilled/heated water loop. A photograph of the test setup is shown in Figure 4.

3.3. Calibration

The PKC CMOS thermometers and power supply samplers must be calibrated prior to any package characterization tests. The thermometers were calibrated by measuring V_{BE} of the PNPs at multiple known temperatures. The chip and package

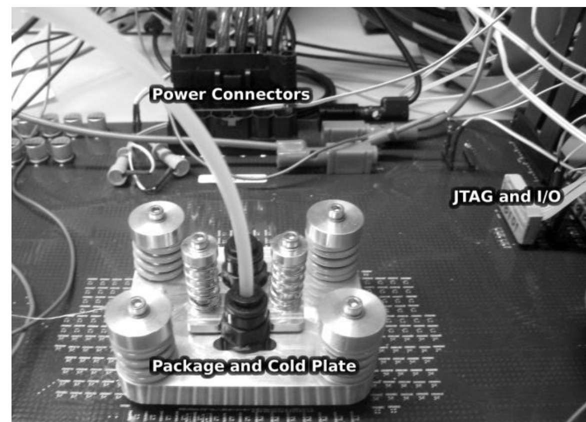

Figure 4. Krazo test setup. Cold plate, I/O, and power connectors are shown.

were insulated on the top and sides with foam and heated from beneath using a hot plate. Discrete resistance thermometers (RTDs) were attached to the package. All on-chip heaters were disabled to minimize heat generated by PKC and the chip was allowed to soak at 25°C for 30 minutes. Each of the on-chip CMOS thermometers' outputs were measured and recorded, along with temperature measurements from the RTD. Calibration was repeated at 60°C and 90°C. The resulting calibration data was used by the test code as a lookup table to interpolate unit cell temperatures during testing.

The on-chip power supply samplers were calibrated using their parallel calibration paths. In this mode, a calibration voltage is sampled rather than the VDD supply. The calibration voltage was swept over the sampler range, 1.6 V to 2.2 V, and the sampler's output was measured and recorded. To account for temperature-dependent effects, such as mobility degradation and threshold voltage shift, calibration was done at 20°C, 30°C, 40°C, and 45°C, by disabling all on-chip heaters, setting the chip water cooling temperature, and recording chip temperature with the CMOS thermometers. The calibration data was used as a 2D lookup table during testing.

3.4. Static Results

For static measurements we applied a constant heat profile to PKC and measured VDD, GND, and temperature in every unit cell. Figure 5 shows a plot of VDD with no heaters turned on, but with the heater shift register clock running. The full range of VDD measured was 1.791 V to 1.797 V. However, the plot contains a smaller range (0.5 mV) to demonstrate the precision of the static measurements. Some single unit cells have a noticeably lower supply voltage compared to their immediate neighbors. These unit cells correspond to the locations of the heater shift register clock drivers. The pattern shows the H-tree structure of the clock distribution. This measurement shows the sensitivity of the static measurements because the clock drivers draw as little as 30 mA peak resulting in droops as small as 0.5 mV.

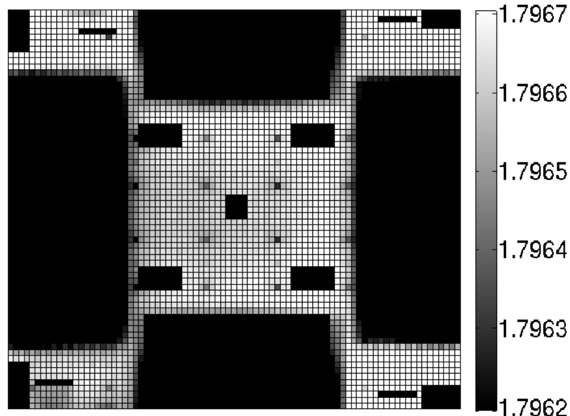

Figure 5. Static VDD measurement with heater clock activated but no active heaters. Voltages below 1.7962 V are compressed to emphasize droop from clock drivers.

Figure 6 shows the measurements from a constant heat profile, where each unit cell is set to draw 27 mW for a total of 106 W. Figure 6(a) shows the supply droop resulting from this heater profile. The droop is most severe in the middle of each chip edge. This is because these areas are depopulated of C4 bumps to allow adjacent chips to overlap PKC as required by proximity communication. The Krazo package allows proximity communication on the east and west sides of PKC, so more C4 bumps are depopulated in those regions. The reduced C4 bump coverage causes the supply droop to be worse on the east and west edges of PKC, as can be seen. Figure 6(b) shows the temperature profile. The temperature is higher in the areas with severe power droop. The heaters in these regions are drawing a similar amount of current as elsewhere on PKC, but resistance of the power supply network has increased which leads to

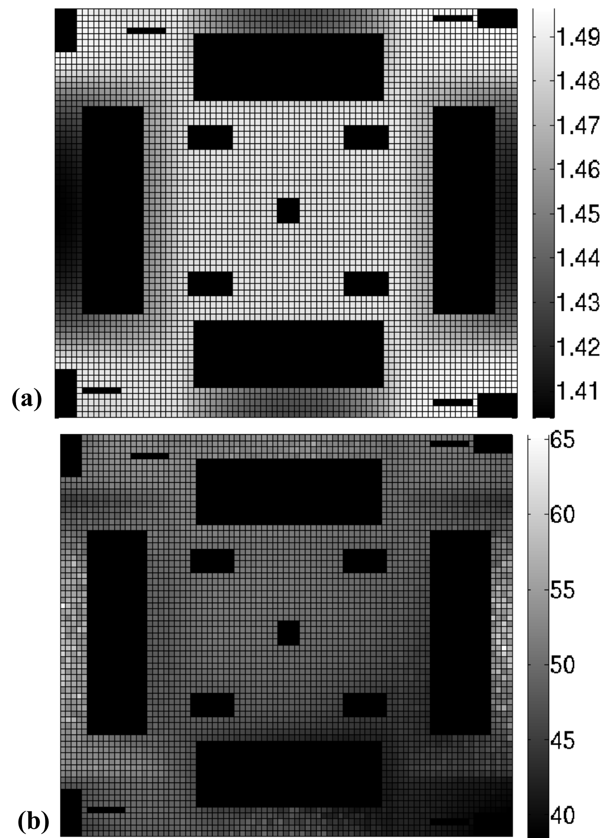

Figure 6. Static VDD, (a), and temperature, (b), measurements with uniform load of 106 W.

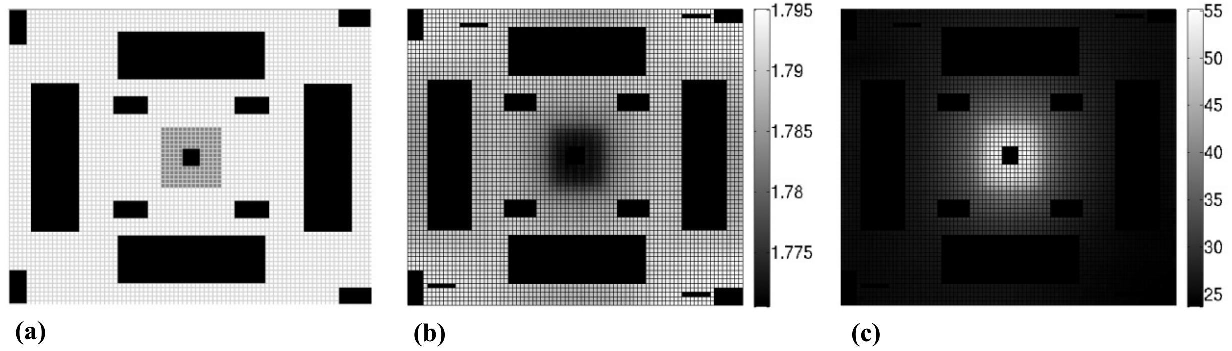

Figure 7. Static measurement results from a hotspot. (a) The gray unit cells are active at 90 µW, all others off. (b) The VDD supply voltage resulting from the hotspot. (c) The thermal profile of the hotspot in ºC.

increased joule heating. A temperature gradient is also visible across the chip, with the southeast corner cooler than the northwest corner. The gradient was attributed to non-coplanar mounting of the chips to the substrate due to varying thickness of the thermal interface material resulting in a better thermal connection to the cold plate in the southeast corner.

Figure 7 shows the static measurements due to a hot spot. To create the hotspot, a grid of 180 unit cells were set to maximum power, 90 mW each, for a total power dissipation of 16.2 W, or 2.55 W/mm^2 as shown in Figure 7(a). This emulates a CPU structure, such as a floating point unit, running at full utilization. Figure 7(b) and (c) show a maximum supply droop of 25 mV and maximum temperature of 55ºC, respectively.

Table 1 summarizes the mechanical characterization results. Krazo does not have structures to characterize the relative orientation of PKC and the package. The data shows the relative orientation of PKC and the overlapping bridge chip. Two measurement sites on the west side of PKC overlap the bridge. The measurements obtained from the on-chip electrical structures is compared to measurements obtained using an IR microscope. The results match well taking into account the 2 µm resolution of the verniers and the error in the IR measurements.

Site	ΔX_{IR}	ΔX_{EL}	ΔY_{IR}	ΔY_{EL}	ΔZ_{IR}	ΔZ_{EL}
SW	6	8	16	14	6	4
NW	7	8	3	6	5	4

Table 1. Mechanical characterization data for electrical and infrared measurements. All units are in µm.

3.5. Dynamic Results

The power supply samplers allowed us to measure and visualize transient voltages on the VDD supply. For the following measurements, the heater shift register clock ran at 500 MHz. A full heater profile period consists of four clock cycles, and is therefore 8 ns long. Each figure depicts the full 8 ns profile.

Figure 8 shows the VDD transients when only the shift register clock is running, but no heaters are activated. The supply droops each time the clock drivers fire. The supply droop waveform is not a single pulse on the clock edge possibly due to drivers in different levels of the clock tree firing at slightly different times in the vicinity of the sampler.

Figure 9 show power supply transients due to the pattern in Figure 7(a). The pattern in Figure 7(a) is applied for a single heater shift register clock cycle, and all heaters are deactivated for the remaining three cycles. Figure 9(a) is from a sampler in the center of the chip amongst the activating heaters. The figure depicts a large droop beginning at the rising edge of the clock that activates the heaters. Figure 9(b) is from a sampler in the southeast corner of the chip observing the same event. In the figure the droop is smaller and occurs about 2 ns after the clock edge that activates the heaters. Further measurements indicate that the second sampler is measuring the

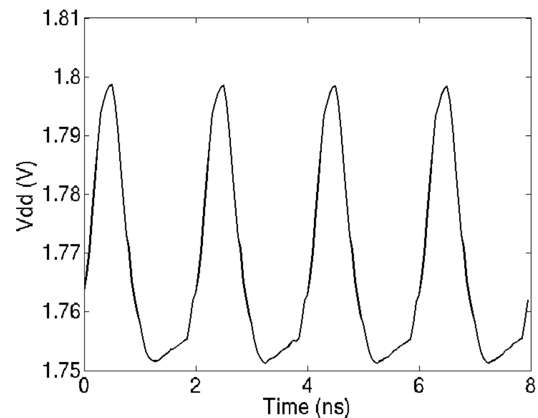

Figure 8. Sampled VDD transient with heater clock activated and no active heaters.

power supply ripple due to the heating event and the ripple velocity across the power grid.

4. Summary

In addition to the test platform presented in this paper, several specialized versions of PKC were developed. One is the bridge chip mentioned earlier in the paper. The bridge chip also contains unit cells, but is lower power and does not have dynamic measurement capabilities. There is also an I/O characterization chip that includes the I/O characterization features described in Section 2.9 in many more unit cells. This allows the characterization of many I/O structures on in a single package, but reduces the amount of VDD and GND I/O resulting in lower peak power dissipation.

The variety and sensitivity of PKC's package characterization circuits permits the complex evaluation of a package with a single chip. With PKC, a package can be subjected to thermal cycles while the mechanical integrity is continuously monitored using the built-in sensing circuitry. This eliminates the need for complex equipment or destructive measurements. Temperature and power supply effects can be correlated due to the presence of both types of measurement circuits side-by-side. A package's ability to deliver clean power under changing loads can be evaluated with the combination of the dynamic heat profiles and power supply samplers. The need for complex MCM packages with increasing power and thermal demands requires simpler ways to evaluate the packages, particularly at the prototyping stage. Combining many measurement capabilities in a single test chip is one way to simplify package evaluation.

PKC has been used to evaluate the first generation of prototype proximity communication packages at Sun Microsystems, with six follow-up packages planned. Additionally, features from PKC will be included on future prototype proximity communication chips to aid package evaluation.

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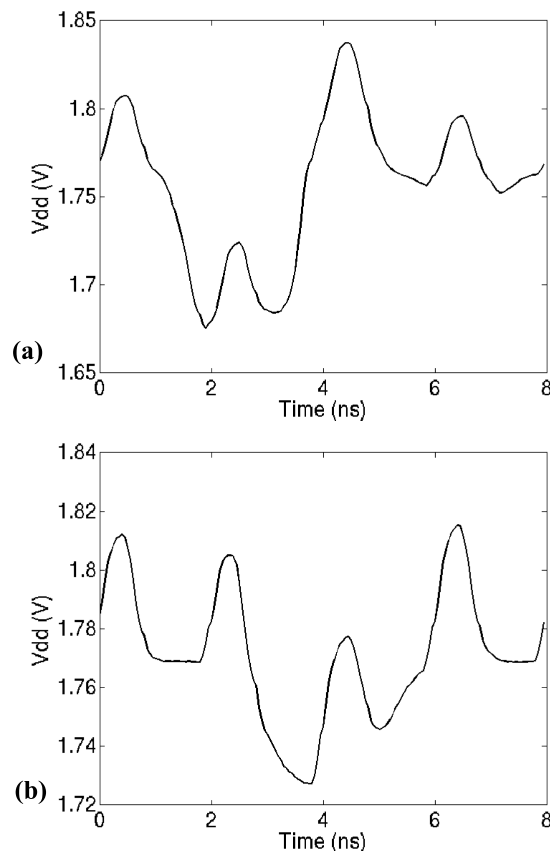

Figure 9. Sampled VDD transient with hotspot in center of chip. (a) Sampled from center of chip. (b) Sampled from corner of chip.

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