A Package Demonstration with Solder Free Compliant Flexible Interconnects.

I. Shubin*, A. Chow, J. Cunningham, M. Giere, N. Nettleton, N. Pinckney, J. Shi, J. Simons, R.Hopkins, J.Mitchell, D. Douglas
Oracle, 9515 Towne Centre Drive, San Diego, CA USA 92121

E. M. Chow, D. DeBruyker, B. Cheng, G. Anderson
Palo Alto Research Center (PARC), 3333 Coyote Hill Road, Palo Alto, CA USA 94304

*(858) 625-5072, ivan.shubin@oracle.com

Abstract.

Flexible, stress-engineered spring interconnects are a novel technology potentially enabling room temperature assembly approaches to building highly integrated and multi-chip modules (MCMs). Such interconnects are an essential solder-free technology facilitating the MCM package diagnostics and rework. Previously, we demonstrated the performance, functionality, and reliability of compliant micro-spring interconnects under temperature cycling, humidity bias and high-current soak. Currently, we demonstrate for the first time the package with the 1st level conventional fine pitch C4 solder bump interconnects replaced by the arrays of micro-springs. Dedicated CMOS integrated circuits (ICs) have been assembled onto substrates using these integrated micro-springs. Metrology modules on the ICs are designed and used to characterize the connectivity and resistance of each micro-spring site.

Introduction.

Current trends and progress in microelectronics continue to be enabled by chip packaging technologies. As die sizes, I/O count, and power densities grow, significant challenges develop in connecting chips to their first-level packages. Additionally, ongoing developments in 3D integration and multi-chip modules (MCMs) present new opportunities for novel I/O technologies that improve performance despite severe dimensional constraints.

Electronic packaging based on stress-engineered spring interconnects [3, 12] can potentially improve chip testing, rework, and mechanical compliance. With conventional flip-chip bonding, the rigid solder reflown microbumps can cause package failure due to excessive shear, as there is a significant CTE mismatch between a silicon integrated circuit (IC) die and the package substrate. Spring-based interconnects, on the other hand, are flexible and compliant; they present a stress-free, lead-free packaging solution for connecting an IC die to ceramic and organic substrates. They also provide rematable connections to enable a reusable, reworkable MCM platform where an ability to separate non-functional and functional die, *i.e.* identifying known good die (KGD), is key to enhancing assembly yield.

Previously, we have realized micro-spring prototypes that meet the stringent electrical and mechanical demands of a typical modern, high-performance microprocessor package; each spring provides <100 mΩ per connection and >30 μm of compliance; spring reliability was also confirmed under 0–100°C temperature cycling, 85/85 temperature humidity bias, and a high-current soak [1-2].

The micro-springs are lithographically-defined metal cantilever beams which self-assemble on the wafer level during fabrication. Beams are sputter deposited with large initial stress gradients. When a spring is released from the substrate, the stress relaxes and its tip lifts off of the substrate plane, becoming a 3D-compliant interconnect that can be compressed against a matching metal pad to form an electrical contact. In previous work we have demonstrated high density gold-gold pressure contacts at 6μm for a laser bar array [4], and at 20 μm pitch for an LCD driver chip [12]. Soldered springs have also been demonstrated for chip to board applications such as memory [3]. The fabrication approach has also been used to build high quality factor coils [5], large angle MEMS actuators [6], and tall tip atomic force microscopy tips [7].

We have transferred the interconnect spring technology onto two types of standard electronic substrates. Fine-pitch substrates with ceramic or organic built-up layers have been populated with high-density arrays of micro-springs; these provide electrical connections to one or multiple silicon CMOS ICs housed within the package. Each IC contains metrology circuits that allow us to measure the connectivity and resistance of each individual spring [10].

In this paper, we report on the development of the microfabrication process that for the first time enables the integration of compliant, fine pitch micro-spring interconnects with ceramic and organic substrates. We show a semiconductor IC packaged onto a substrate using these interconnects, describe assembly details, and present the metrology results.

1. Micro-spring processing.

Fabricating thin film structures onto ceramic or organic substrate requires careful surface preparation. The spring fabrication process uses sputtering and plating of thin films as well as photoresist based lithography, so smooth planar substrate surfaces are required for high yielding process. The two reported substrates are of ceramic and organic build up layers. Both types of substrates have their pros and cons. Ceramic ones have higher thermal conductivity, closer to

silicon CTE, while organic ones are more compact and cost effective, their design rules are more relaxed. We are experimenting with both types in order to identify which one would prove superior to integrate with micro-spring interconnects from the performance and manufacturing standpoint.

Our substrates are 45mm×45mm and are designed to package two flipped 15mm×12mm active chips "bridged" with a third one which establishes capacitive proximity communication (PxC) between the first two [9]. There is an allocated cavity in the substrates to accommodate the bridge chip. The substrates' dimensions and the PxC technology background have been detailed earlier [8, 9]. The ceramic substrate is built out of 16 alumina layers with tungsten conductors in the top layer arrayed at 180µm pitch on the chip side and at 1 mm pitch on its LGA socket side. Organic substrates are entirely identical in their layout to the ceramic ones but built with copper conductors. The C4 landing pads are on a 180µm pitch for both types of substrates and have been finished with Ni/Au metallization. The basic schematic substrate view of the top surface is pictured in Figure 1.

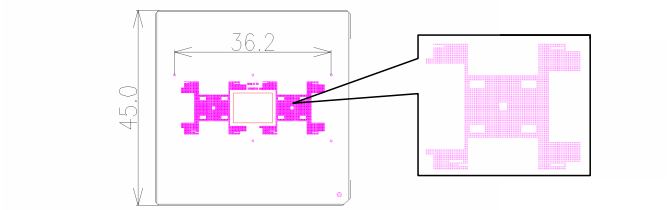

Figure 1. A schematic view of the top substrate surface showing sites for two 15×12mm^2 chips. The callout zooms into one of these sites with 2200 landing pads.

The overall sequence of micro-spring fabrication steps is demonstrated in Figure 3. The "as manufactured" ceramic or organic substrates are initially not fully compatible with thin processing, because the solder bumps and under bump metallurgy (Ni/Au) are elevated above the surface while the alumina ceramic top surface is also too rough. Both types of substrates have been characterized on planarity and found to have on average about 90 µm and 30 µm of overall surface variation, non-planarity, for ceramic and organic substrates respectively. To planarize and smooth the surface out, the substrates were polished, resulting in a local roughness of less than 0.1 um and step heights of <0.5 µm near tungsten or copper vias. However, the original granularity of the ceramic substrate remained, resulting in many 2 µm deep holes. To address this non-uniformity and to ensure adequate metal thin film adhesion, a spin-on dielectric, benzocyclobutene (BCB), is applied to the substrates for planarization. The BCB is intended to achieve about 1 µm thin films. Figure 2 displays a fragment of the pre-BCB planarized ceramic surface after polishing step.

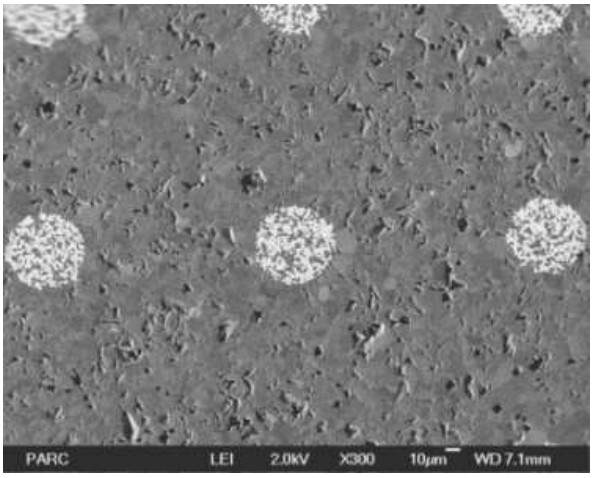

Figure 2. SEM micrograph of the top ceramic substrate surface after polishing. Tungsten filled vias are shown on the 180 µm pitch.

Next, photoresist lithography and etching are used to open up the BCB dielectric over the vias (Figure 3b). The substrates are then placed in a sputtering tool to deposit a release layer (Ti) and spring metal stack (Au-MoCr-Au). The stress in the MoCr is controlled such that there is a vertical gradient of intrinsic stress ranging in magnitude from a GPa compressive to a GPa tensile. The spring metal stack is patterned with photolithography to form the spring anchor, body and tip (Figure 3c). Another photoresist mask is spin-coated and patterned to define spring release regions. A selective wet etch is then used to extract the release titanium layer underneath the spring and allow the stress to relax, so that each spring lifts its body out of the deposition plane and self-assembles. Finally the springs are plated with additional metals (Au) for extra strength and conductivity (Figure 3e). Each spring is 100 µm long, 30 µm wide and 3.5µm thick. The tip is originally 45 µm above the surface (Figure 3e).

The spring contacts are arranged on a 180µm×180µm pitch array (Figures 4, 5). The pattern matches a dedicated test chip specially designed for contact resistance measurements and spring yield as well as proximity communication (PxC) experiments. The substrate has a cavity to house "bridge" chips and facilitate future proximity packaging demonstrations. Achieving high yield lithography around this cavity requires careful attention to the photoresist coating uniformity.

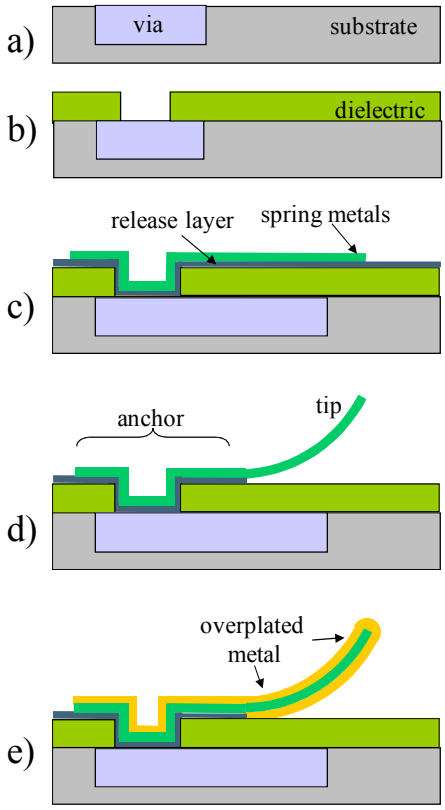

Figure 3 . Micro-spring fabrication process flow.

Close-up images of the contacts show the circular tungsten filled via underneath the rectangular spring anchor (Figures 6, left and right). The position of the tungsten filled vias is not registered well on the 180 µm pitch array with respect to the GDS layout because of the thermal runout inherent in the substrate co-firing fabrication process. Tungsten filled vias are visible to the left side of the spring anchor (Figure 6 left). Each contact site is a dual micro-spring structure. Therefore a dimensional correction to the micro-spring mask layout may be required in order to properly position micro-springs onto each of the substrate's via site across its entire footprint.

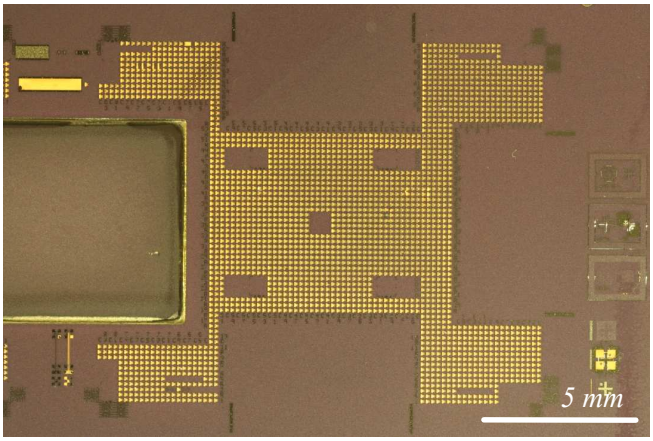

Figure 4. Optical microscope micrograph of the array of micro-springs fabricated on the ceramic substrate.

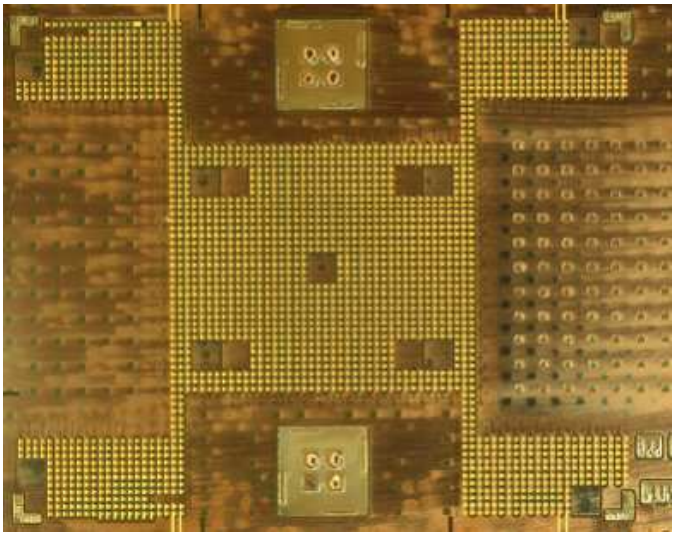

Figure 5. Optical microscope micrograph of the array of micro-springs fabricated on the organic substrate.

Organic substrates have been found to have much improved feature registration with acceptable deviation of copper via landing pad locations with respect to the original GDS layout (Fig.7). It insures proper micro-spring positioning across the substrate and simplifies interconnect designs for multiple chip packaging.

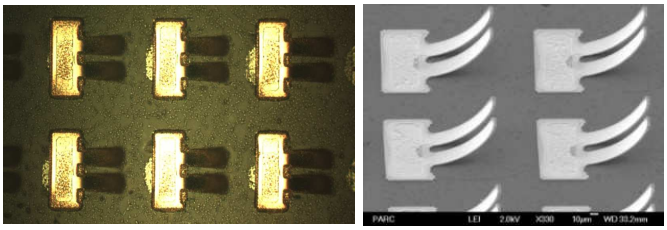

Figure 6. Left: optical image of the top view of the processed micro-springs on the ceramic substrate. Right: SEM micrograph showing lifted-off dual micro-springs on every via site.

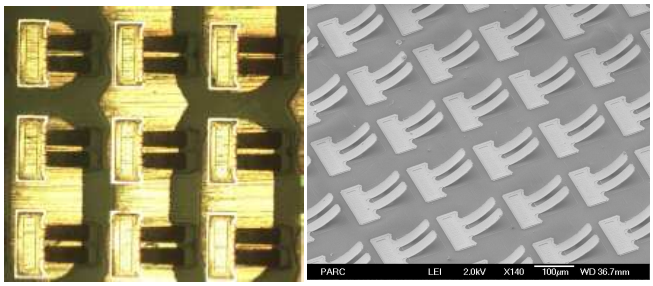

Figure 7. Left: optical image of the top view of the processed micro-springs on the organic substrate. Right: SEM micrograph showing the lifted-off dual micro-springs on every via site.

2. Package Assembly.

An active IC was flip chip assembled onto ceramic and organic substrates with springs to form the package (Figure 8). In the current micro-spring interconnect demonstration only one chip was assembled onto each of the substrates. The chip's aluminum C4 pads were finished with Ni/Au by electroless plating. The silicon IC has incorporated four corner etch pits each housing a precision spacer glass ball. In previous work, matching pits in another substrate were used to enable very precise 3D alignment of chips (with tolerances below +/- 2 µm) while only requiring a coarse (>50 µm) alignment accuracy from assembly tools [1, 13]. In this work, the ceramic and organic substrates do not have matching pits, so the balls are used only to establish an accurate gap. A ball diameter of 135 µm was selected to reside on the bottom of the 95 µm deep etch pit. By design, the gap between the ceramic/organic substrate and flipped IC top surface is targeted at 20 µm. For this spring design, this corresponds to a spring compression of 25 µm. Previous four-wire measurements of resistance versus compression suggest that this puts the spring well into the resistance plateau region where the resistance is insensitive to amount of further compression [7].

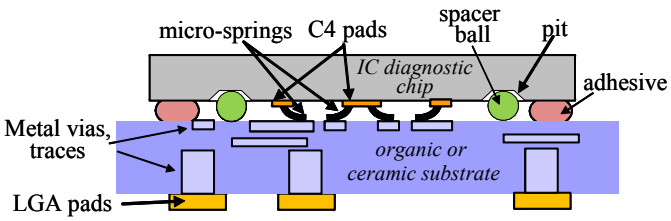

Figure 8. Schematic cross-section of the assembled micro-spring package.

The flip chip optics and assembly process need to provide the x-, y- alignment. The IC contact pads are 80 µm with a 70 µm window in top passivation layer. The spring pair is 60 µm wide, so the alignment error should be less than +/- 5 µm to ensure that both tips are entirely situated on the pad. If one of the two tips is half off the pad (Figure 9), the effective tip-pad interface area will decrease by 25%, but the overall resistance increase should be less than 10 mΩ. Essentially, the micro-springs' performance can tolerate IC to the substrate misalignment on the order of +/- 12.5 µm in line with current flip chip assembly tooling. This estimate is based on previous modeling of the contact which suggested that the sum total of the resistance due to the tip-pad contact area of both tips is ~10-40 mΩ. The total spring contact resistance is 70-100 mΩ, consisting of the sum of contributions from the tip-pad area, spring body, spring anchor and pad spreading, suggesting this misalignment increase the total resistance by <10% [7]. Future packages can be designed to readily provide improved relaxed alignment tolerances without sacrificing the interconnect contact resistance.

After aligning the springs to the IC pads, the IC is lifted and compressed at least three times to pre-scrub the tip and pad surfaces. This has been found to lower the resistance 5-20 % [7]. Before the final compression, adhesive is placed on the edges of the packages and UV cured around the edge of the chip. Thermal cures have previously been used for spring assemblies and may be implemented in future assemblies. Figure 10 shows completed finished package assemblies. Understandably the adhesive permanently locks the chip down while in order to benefit from the micro-spring interconnect rework capability one would need to deploy a clamping mechanism facilitating both package assembly and des-assembly similar to that shown in [1]. Adhesive has been utilized in this work in order to secure the chip on the substrate to expedite the demonstration of the spring interconnect operation and performance. Truly reworkable packages are development.

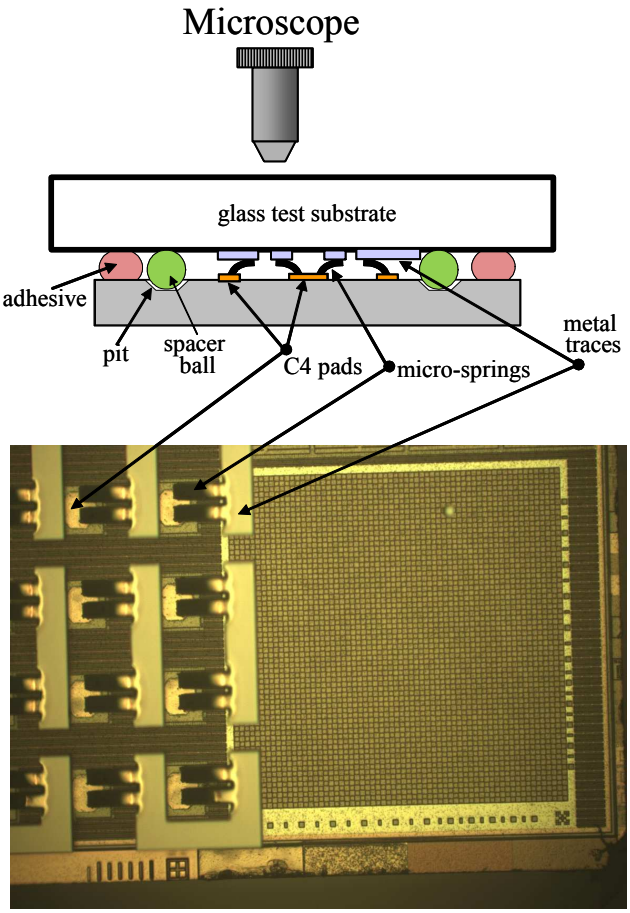

Figure 9. Top OM view image of microspring tips aligned and assembled to the IC pad chip. In this practice assembly the springs were first fabricated on the glass substrates, enabling direct visual inspection of the assembly. The springs are misaligned by 15-20 µm in the y-direction, causing one of the two tips to land outside of the pad window, which should not effect the total resistance by more than 10%.

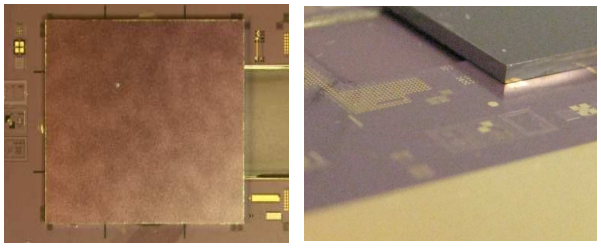

Figure 10. Assembled packages displaying attached IC chip on the ceramic substrate. Left: top view (IC chip face-down). Right: angled view.

3. The Test IC Chip.

To study the yield and electrical characteristics of micro-spring (and other types of) connections, we built a test chip with metrology circuits that characterize the thermal, electrical, and mechanical properties of various packages [10]. If used with a proper cooling and power delivery system, the test chip can also dissipate up to 355W of power at 1.8V; this simulates the thermal profile of a typical high-performance microprocessor, and allows us to study the performance of packages under these extreme thermal loads. For this reason, the test chip was code named the "Package Killer" chip (PKIC). Note, however, that we did not exercise the full power dissipating capability of the PKIC, as the micro-spring test setup was not designed to deliver high power or remove the resulting heat.

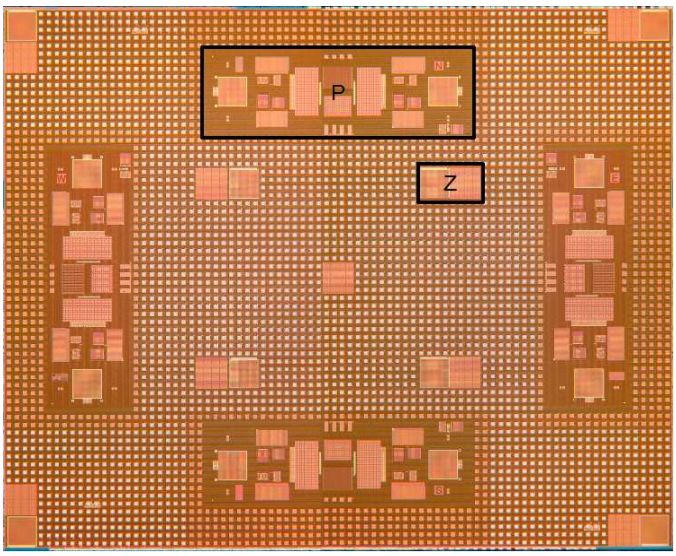

Figure 11. Die photo of the Package Killer IC (PKIC).

The PKIC was fabricated in a 0.18 μm, 6-layer Aluminum metal, CMOS technology. The chip (Figure 11) has a relatively large footprint of 15mm×12.5mm. The nine small rectangular structures (labeled "Z") at the center and corners of the chip are sensor structures used to measure the separation between the chip and the substrate [11]. The four large rectangular structures (labeled "P") along the four sides of the chip are used for chip-to-chip data communication [9], and are not relevant to the experiments described herein. Their functionality will be tested in the future work.

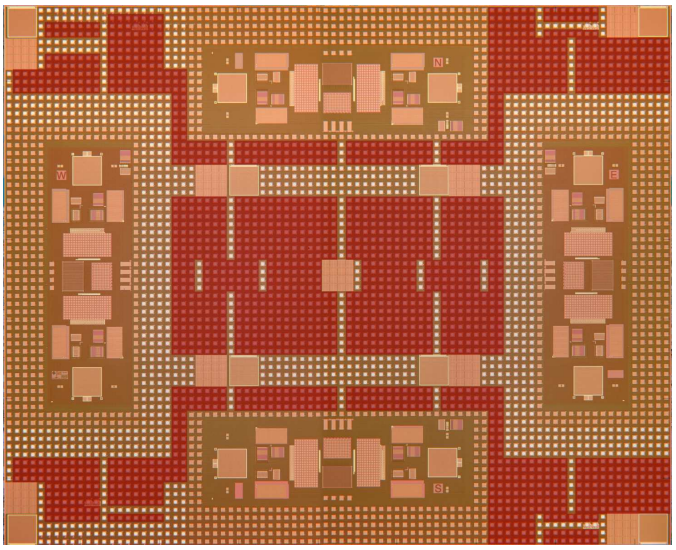

Figure 12. PKIC top view with highlighted 1702 unit cells used in the micro-spring characterization.

The remainder of the PKIC consists of an array of unit cells. There are 3944 such cells, spaced on a 180 × 180 μm^2 pitch (Figures 11, 12). A unit cell consists of a C4 bump site that can connect to the substrate via a pair of micro-springs. There are several different types of unit cells. Some contain on-chip thermometers that can measure the temperature of the chip at that location; some contain sensors for detecting the supply voltages; some carry sampling circuits for probing on-chip supply waveforms to characterize noise under dynamic loads [10].

Of particular interest to the experiments described here are unit cells with metrology circuits that can measure the connectivity and resistance of an individual spring connection. 1702 such unit cells were used to characterize their corresponding spring connections, as shown in Figure 12.

Figure 13 shows the metrology circuit in each unit cell. It determines the connectivity of each spring connection and measures its resistance through a 3-wire method. Each circuit consists of two switches, both connected to the bond pad where a connection to a micro-spring can be formed. One switch is part of the current network, while the other is part of the voltage network. Both networks are shared across all unit cells on the chip, and are connected to the substrate through other micro-springs at several different dedicated sites on the chip (for redundancy).

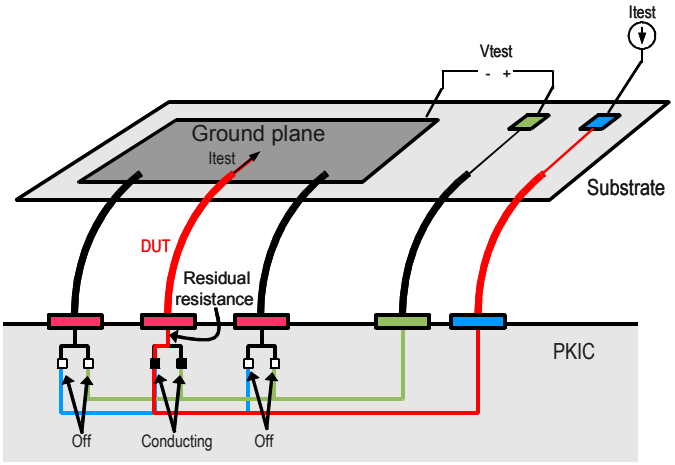

Figure 13. 3-point measurement of micro-spring resistance.

To measure the resistance of a particular micro-spring connection, the pair of switches at the location under test are closed (or shorted), and the switches at all other locations are opened. A known test current, I_{test}, is driven onto a current network from the substrate. This current travels through a micro-spring onto the PKIC, through a switch in the unit cell at the location under test, and back to the substrate through the micro-spring under test (DUT), the resistance of which is being measured. As it is infeasible to have a dedicated return pin on the substrate for every connection, this return pin is shared among all the test sites, and is either the power (VDD) or ground (GND) plane.

To perform the 3-point resistance measurement, we probe the voltage between the return pin (VDD or GND) and a voltage network on the substrate. Ideally, no current flows through this voltage network, so the voltage of the network on the substrate should correspond to that at the bond pad. The value of V_{test} should therefore indicate only the voltage drop across the micro-spring under test (DUT) and the return pin. Unlike a 4-point method, this 3-point measurement includes the undesired resistance of the return pin; however, since it is a ground plane on the substrate, its resistance is typically low. The resistance of the DUT is then simply $R_{DUT} = V_{test} / I_{test}$.

4. IC/micro-spring/substrate package characterization.

The package assemblies based on ceramic and organic substrates have been characterized according to the described technique in order to evaluate micro-spring contact resistance and yield. The same PKIC chips with solder bump arrays in place have been flip chip bonded onto identical ceramic and organic substrates in order to provide a reference for direct initial comparison of micro-spring interconnects to the conventional solder bump interconnects.

Figures 14 and 15 are color maps showing the measured spring resistance at each of the 1702 interconnect sites on a ceramic and an organic substrates, respectively. Some sites on the chip are used for other purposes (*e.g.* data communication, alignment measurement, power delivery) and hence contain no metrology circuitry; these sites have no corresponding resistance data and are shaded black. Both plots have been obtained with the very first built prototypes, and are not statistical averaged results obtained from multiple experiments.

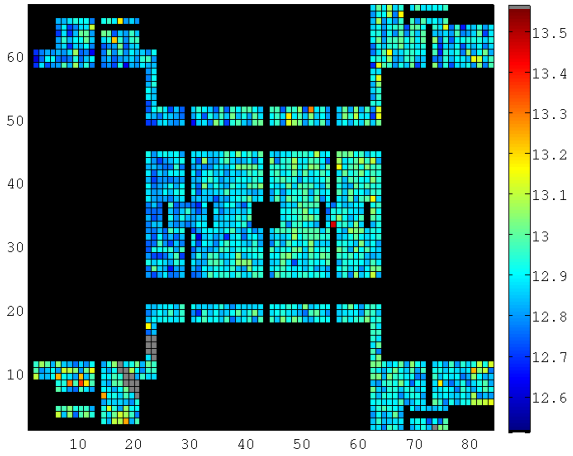

Figure 14. Micro-spring resistance and yield color map of the ceramic substrate based package for 1702 tested interconnects.

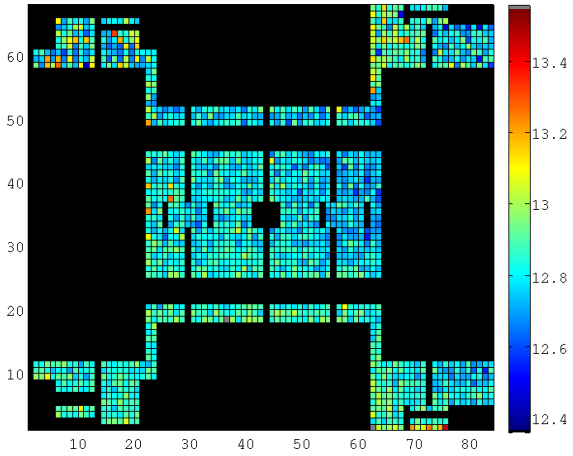

Figure 15. Micro-spring resistance and yield color map of the organic substrate based package for 1702 tested interconnects.

The mean resistance values for an individual interconnect site are 13.1 Ω and 13.2 Ω for the ceramic and organic substrate assemblies with micro-springs, respectively. The micro-spring yields are 99.9% and 98.9% for the ceramic and organic builds, respectively; only the open connections are considered failing. Some yield deviation from 100% on the micro-spring packages is attributed to defects in micro-spring production which are being addressed with improved microfabrication processes. 100% yield spring fabrication for

this identical layout was demonstrated previously on silicon substrates [1, 2].

For the packages with conventional reflown solder. the mean average resistances measured 11.7 Ω and 11.8 Ω for the ceramic and organic substrates, respectively, with 100% yielding sites.

The raw measured data includes the residual resistance of any wire trace that connects the switches to the bond pad (Figure 13). (In fact, it also includes the resistance of the bond pads and any resistance in the supply network on the substrate, but these resistances are negligible). The residual resistance of these on-chip wire traces is significant (approximately 12 Ω) and largely dominates the spring resistance being measured. Differences in measured resistance between the soldered and micro-spring interconnects are largely due to on-wafer and wafer-to-wafer variability in the IC metal trace resistance. This variation is approximately 10% for this lot, and can explain the observed resistance discrepancies between the solder and micro-spring interconnected chips. The results are consistent with our expectation that the micro-spring contact resistance is <0.1 Ω, in accordance with previous demonstrations [1].

Conclusions.

We have successfully fabricated flexible micro-springs on the fine 180 μm pitch on both ceramic and organic substrates and demonstrated electronic packages of large foot print high I/O count die. For the first time the conventional C4 solder bumps have been replaced with compliant interconnects on the electronic substrate facilitating package and rework required for low cost MCM production. The micro-spring interconnects have been characterized and found to have high process yield and low electrical resistance.

Acknowledgments.

PARC acknowledges Lai Wong and Jim Zesch for processing support. Oracle acknowledges the Advanced Packaging team in the Microelectronics group for their packaging effort, and the VLSI Research group in Sun Labs for the design of the Package Killer IC.

References

1. I. Shubin, E. M. Chow, J. Cunningham, D. De Bruyker, C. Chua, B. Cheng, J. C. Knights, K. Sahasrabuddhe, Y. Luo, A. Chow, J. Simons, A. V. Krishnamoorthy, R. Hopkins, R. Drost, R. Ho, D. Douglas, and J. Mitchell, "Novel packaging with rematable spring interconnect chips for MCM", 2009 IEEE 59th Electronic Components and Technology Conference (ECTC 2009), 26-29 May 2009, Piscataway, NJ, USA, 2009, pp. 1053-1058.
2. B. Cheng, E. M. Chow, D. DeBruyker, C. Chua, B. Cheng, K. Sahasrabuddhe, I. Shubin, J. Cunningham, Y. Luo, A. V. Krishnamoorthy, “Micro-Springs for Microprocessor IC Packaging and Testing”, Proceedings of the 42nd International Symposium on Microelectronics, 2009.
3. E. M. Chow, D. K. Fork, C. L. Chua, K. Van Schuylenbergh, and T. Hantschel, “Wafer-level packaging with soldered stress-engineered micro-springs,” IEEE Transactions on Advanced Packaging, vol. 32, 2009, pp. 372-378.
4. C. L. Chua, D. K. Fork, and T. Hantschel, "Densely packed optoelectronic interconnect using micromachined springs", IEEE Photonics Technology Letters, vol. 14, 2002, pp. 846-848.
5. C. L. Chua, D. K. Fork, K. Van Schuylenbergh, and J. P. Lu, "Out-of-plane high-Q inductors on low-resistance silicon", Journal of Microelectromechanical Systems, vol. 12, 2003, pp. 989-995.
6. M.A. Rosa, D. De Bruyker, A.R. Volkel, E. Peeters, and J. Dunec, “A novel external electrode configuration for the electrostatic actuation of MEMS based devices”, IOP Journal of Micromechanics and Microengineering 14, 2004, pp. 446-451.
7. T. Hantschel, E. M. Chow, D. Rudolph, D. & D.K. Fork, “Stressed metal probes for atomic force microscopy,” Applied Physics Letters 81, 14 Oct. 2002, pp. 3070-3072.
8. T. Sze, M. Giere, B. Guenin, N. Nettleton, D. Popovic, J. Shi, S. Bezuk, R. Ho, R. Drost, and D. Douglas, “Proximity Communication Flip-Chip Package with Micron Chip-to-chip Alignment Tolerances”, 2009 IEEE 59th Electronic Components and Technology Conference (ECTC 2009), 2009.
9. R. Drost, R. Hopkins, R. Ho, I. Sutherland, “Proximity Communication,” IEEE Journal of Solid-State Circuis, vol. 39, Sep. 2004, pp. 1529-1535.
10. J. Schauer, N. Pinckney, N. Nettleton, D. Popovic, “A Test Platform for the Thermal, Electrical, and Mechanical Characterization of Packages,” Proceedings of the 42nd International Microelectronics and Packaging Society (IMAPS), 2009.
11. A. Chow, R. Hopkins, R. Ho, R. Drost, “Measuring 6D Alignment in Multi-Chip Packages,” 6th Annual IEEE Conference on Sensors, 28-31 Oct. 2007, pp. 1307-1310.
12. E. M. Chow, C. Chua, T. Hantschel, K. Van Schuylenbergh, and D. K. Fork, "Pressure contact micro-springs in small pitch flip-chip packages," IEEE Transactions on Components and Packaging Technologies, vol. 29, 2006, pp. 796-803.
13. J. E. Cunningham, X. Zheng, I. Shubin, R. Ho, J. Lexau, A. V. Krishnamoorthy, M. Ashari, D. Feng, J. Luff, H. Liang, and C.-C. Kung, “Optical Proximity Communication in Packaged SiPhotonics,” Proceedings of 5th International Conference on Group IV Photonics.